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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of : DAVID L. ISAMAN  
Serial No. : 09/443,160  
Filed : November 19, 1999  
For : SYMBOLIC STORE-LOAD BYPASS  
Group No. : 2183  
Examiner : Daniel H. Pan

**BOX FEE AMENDMENT**  
Commissioner for Patents  
Washington, D. C. 20231

Sir:

**PROPOSED AMENDMENT TO THE DRAWINGS**

The Examiner is respectfully requested to approve the amendments to the drawings of the above-identified application. Please amend Figure 2A as shown in the attached drawing copies.

Figure 2A has been amended to add reference numeral 200. This change was made to make the drawings correctly reflect the text of the specification at Page 10, Line 13. Therefore, no new matter has been added by adding reference numeral 200 to Figure 2A.

Figure 2A has also been amended to correct original reference numeral 115 (in block 214) to read 215. This change was made to make the drawings correctly reflect the text of the specification at Page 11, Line 18. Therefore, no new matter has been added by correcting reference

numeral 115 to reference numeral 215 in Figure 2A.

The proposed amendments have been entered in red on the attached drawing cop  
facilitate review by the Examiner. Upon approval, the drawings will be amended by an auth  
commercial bonded drafting firm. If any outstanding issues remain, or if the Examiner ha  
suggestions for expediting allowance of this Application, the Applicant respectfully invite  
Examiner to contact the undersigned at the telephone number indicated below o  
[wmunck@davismunck.com](mailto:wmunck@davismunck.com).

Respectfully submitted,

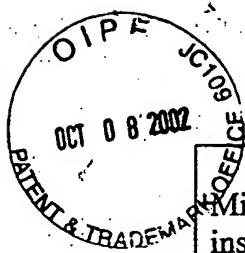
DAVIS MUNCK, P.C.

Date:

Oct. 3, 2002

  
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200

210  
Microprocessor is coupled to an instruction memory 150 which includes a plurality of instructions 151, and is ready to perform those instructions 151.



211  
The microprocessor reads a sequence of instructions 151 from the memory 150 using instruction fetch stage 110.



212  
Instruction fetch stage 110 couples the instructions 151 to the instruction decode stage 120.



213(a)  
The instruction decode stage 120 parses the instructions 151 to determine whether they are instructions to load data to an external memory or store data from an external memory.



213(b)  
The instruction decode stages 120 determines the syntax of any addresses in the external memory that the instructions 151 refer to as operands.



214  
The bypass element 121 examines parts of the instruction 151, including information about what operations the instructions 151 command the microprocessor 100 to perform. If these operations are to load or store data, the method continues with step ~~215~~. If these operations are otherwise, the method continues with step 221.

META-01<sup>a</sup>  
Fig. 2A

215  
A record of the symbolic operands store operations to external memory stored in a table that is indexed by the instruction ID.



216  
Each load instructions' operands are compared against the store instructions being issued in the ongoing clock cycle and those of all unretired store instructions.



217  
The bypass element 121 determines whether the operand addresses that the instructions 151 refer to include identical base address values. If so, the bypass element generates a bypass signal. If not, the bypass element does not generate a bypass signal.



220  
The microprocessor can act on the knowledge that the instructions 151 refer to identical locations in an external memory.



221  
The instruction decode stage 120 couples the parts of the instruction 151, including information about the base address value and the offset address value to the address computation stage.



215 TO FIG 2B